	US ATLAS **PHASE II Upgrade** **BASIS of ESTIMATE (BoE)**	**Date of Est:** **10/19/2015** **Prepared by:** **John Parsons** **Docdb #:**

WBS number: 6.4.2.2 (LArFE_Columbia)	**WBS Title: LAr FE Electronics at Columbia University**

WBS Dictionary Definition:
This WBS covers the effort at Columbia University Nevis Laboratories on the design and fabrication of frontend readout electronics for the LAr calorimeter system.

The deliverables for WBS 6.4.2.2 are 1627 Frontend Boards (FEB2), each instrumenting 128 channels of LAr calorimetry, and the ~52k custom ADC chips, each instrumenting 4 LAr calorimetry channels, which are needed to fully equip all FEB2. A total of 1524 FEB2 need to be installed to equip the entire LAr calorimeter system, with the additional FEB2 being overages. The costs also include typically 6% overages for all components.

Estimate Type (check all that apply – see BOE Report for estimate type by activity):

___ Work Complete
___ Existing Purchase Order
___ Catalog Listing or Industrial Construction Database
___ Documented Vendor Estimate based on Drawings/ Sketches/ Specifications
_X_ Engineering Estimate based on Similar Items or Procedures
_X_ Engineering Estimate based on Analysis
_X_ Expert Opinion

Supporting Documents (including but not limited to):

Details of the Base Estimate (explanation of the Work)

This BOE covers the engineering, fabrication and testing of the ADC chips and FEB2.

ADC M&S Costs

The ADC chip is being designed in the 65 nm CMOS process available from TSMC. The production cost is based on current estimates, provided by Philippe Farthouat (see attached email), that the NRE cost for production of the full mask set is currently $760k (including 6 wafers delivered). It is assumed that the same production run will be shared by the ADC and also the other 65 nm LAr chips, namely the preamp/shaper and the serializer. In that way, it will only be required to pay the NRE cost for the mask production once. This one-time NRE charge is included in the ADC production cost. In addition, production of each additional 25 wafers costs $85k. The sizes of the ADC, preamp/shaper and serializer chips are not yet known. We include the cost of producing an additional 100 wafers.

The ADC chips will need to be packaged. The cost is estimated based on a quotation from Quik-Pak (see attached) for packaging the ADC chip developed for the Phase I LAr upgrade, namely $6 per chip assuming 10k chips. We

could anticipate some reduction in the per chip cost due to the larger quantity. However, this will be offset at some level by the influence of inflation over the next 4-5 years. Therefore, we have assumed $6 per chip, and a yield of 70%.

Putting this together, the estimated ADC production cost is $760k (NRE) + $340k (100 wafers) + $418k (packaging), for a total of $1.518k. Note that this cost also includes the cost of producing (but not packaging) the LAr preamp/shaper and serializer chips.

FEB2 M&S Costs

The FEB2 is a large multilayer complex printed circuit board (PCB), that includes 32 chips each of the 4-channel preamp/shaper, ADC and serializer, plus additional logic, power regulation and distribution, optical data and control links, etc.

The FEB2 is the same size, and of a similar complexity, as the original FEB, which was also designed by Columbia. Therefore, the cost estimate for the FEB2 uses the knowledge acquired with the original FEB production. The materials cost of the original FEB totaled $5,427k (see attached); this includes production and assembly of 1627 boards, as well as typically 6% overages for parts. This cost does not include the preamps or shapers, nor the optical link components; this is appropriate for comparison with FEB2 since those items are costed separately for FEB2. However, to more precisely compare with the FEB2, one should remove $1,445k for the cost of the SCA (which is not used on FEB2) and also $620k for the ADC (since the ADC chips are costed separately for FEB2). Subtracting these 2 items gives an adjusted cost of $3,362k for the original FEB production, or about $2,100 per FEB. To allow for inflation in the almost 15 years since the production of the original FEBs, we estimate a materials cost for FEB2 of $2,500 per FEB2. For a total of 1627 FEB2s, this totals $4,068k.

More recent cost information can be obtained using the example of the LTDB being designed by BNL for the Phase I upgrade. The cost estimate for the LTDB digital motherboard (see attached) is $1,736 per board for a quantity of 150 boards. One would expect some reduction for a larger quantity. However, the LTDB digital motherboard, while the same size as the FEB and FEB2, has a large portion of its surface essentially empty in order to receive a large analog daughter card that contains all of the analog functionality of the board. As a result, the LTDB digital motherboard is less complex than the FEB2 and also houses fewer components. Given these differences, the LTDB cost supports the assumed cost of $2,500 per FEB2.

The manpower estimate uses experience from the original FEB development. The estimate was developed bottoms-up, and totals 6060k in FY17-FY24 (4403k in FY20-FY24). In comparison, the original FEB development (which also included the SCA chip development) had an actual labor cost of 4217k. The total labor cost FY17-FY24 therefore represents a 37.6% increase over that of the original construction. Given that the workloads are quite similar, the comparison provides confidence in the estimate, given the impact of inflation in the intervening ~15 years.

***still to complete the manpower documentation, plus the various parts coming after this

Schedule:

Assumptions:

Risk Analysis

The risk will eventually be used to assess the contingency. It is important to begin to document this process. In this first iteration, state what are the primary risks to the deliverable to the best of your knowledge. Risks are classified into three categories – Specify them as you see them below.

Schedule Risk:
- Probability:
- Potential Problem:
- Mitigation:

Cost Risk:
- Probability:
- Potential Problem:
- Mitigation:

Technical/Scope Risk:
- Probability:
- Potential Problem:
- Mitigation:

M&S Contingency Rules Applied

50%

Labor Contingency Rules Applied

50%

Comments:

From Philippe Farthouat
Subject **Re: 65 nm question**
To John Parsons
Cc Philippe Farthouat

Reply | Forward | Archive | Junk | Delete | More
10/7/15, 12:25 PM

Hi John,

An MPW run in 65 nm for a 12 mm2 chip costs about 63 kUSD (I think it contains 100 chips).
An MPW run for a 64 mm2 chip costs 320 kUSD

NRE for full mask set and 6 wafers delivered costs about 760 kUSD (2016 price)
NRE when multi layer mask (MLM) is used and 6 wafers delivered: 483 kUSD (2016 price)

Production cost for 250 wafers (no MLM): 802 kUSD (2016)
Production cost for 25 wafers (no MLM): 85 kUSD (2016)

NRE and production costs are for "base technology" i.e. 12" wafers, standard core transistors, 2.5 V IO transistors, 7 metal layers

Might be wise not to circulate these numbers too largely...

Cheers, Philippe

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Quik-Pak™
Microelectronic Packaging & Assembly Solutions

OPEN·molded Plastic Package

Quote#: 10752

Quik-Pak
10987 Via Frontera
San Diego, CA 92127
Ph. - (858) 674-4676
Fax - (858) 674-4681
bill@icproto.com

Name: Nancy Bishop
Company: Columbia Univ. Nevis Labs
Location: NY
Date: 2/20/2014

Budgetary Quote (Conservative): 10,000 pieces

Qty		Description	Unit Price		Line Total
10000		72 Pin 10mmx10mm Air Cavity Assembled QFN	$6.00		$ 60,000.00
		Includes wafer finishing, air cavity package, lid, wire bonding, lid seal and branding			
		TBD TURN			
Note: Pricing above may be revised if scope of work changes				**Subtotal**	$ 60,000.00
				Total	$ 60,000.00

by: *Bill Lawrence*
East Coast Sales Manager

	Assembled FEBs				
		Cost		Spare	FEB
Component	Cost/FEB	Extended	Fixed	Parts	Total
SCA	$837.69	$1,363,007		$81,780	$1,444,788
ADC	$352.64	$573,784		$45,903	$619,687
SCA Controller			$280,000	$0	$280,000
Voltage regulators	$318.71	$518,583		$41,487	$560,069
Config. Controller	$25.85	$42,054		$3,364	$45,418
Gain Selector	$0.00	$0	$40,000	$0	$40,000
Spac Slave	$36.36	$59,168		$4,733	$63,901
SPAC connector	$4.00	$6,508		$521	$7,029
Twin-ax	$4.85	$7,891		$631	$8,523
COTS	$351.17	$571,393		$45,711	$617,104
PC board	$173.00	$281,490			$281,490
preamp RF shield	$17.24	$28,052			$28,052
BP connector shield	$34.88	$56,754		$4,540	$61,294
BP connectors	$12.00	$19,525		$1,562	$21,087
Power connector	$16.24	$26,424		$2,114	$28,538
Power comb	$13.05	$21,234		$1,699	$22,932
Front panel	$50.00	$81,356			$81,356
Ground pins	$15.00	$24,407		$1,953	$26,359
Conductive tapes	$20.00	$32,542			$32,542
Cooling interface	$100.00	$162,711			$162,711
Assembly	$475.00	$772,877			$772,877
TTCrx	$33.14	$53,927		$4,314	$58,241
Reserve	$100.00	$162,711			$162,711
Total cost (FEB)	$2,991	$5,186,397		$240,313	$5,426,710

Cost Estimate of LTDB Digital Mother Board

P/N	Manufacture	Description	Distributor	Qty	Unit Cost	Cost/Board	Contingency	Value
LTDB MB	Many	PCB Fabrication	Many	1	$ 450.00	$ 450.00	50%	$ 225.00
Assembly	Many	PCB Assembly	Many	1	$ 485.00	$ 485.00	50%	$ 242.50
Analog Mezzanine	LAr	40-ch Analog Mezzanine Card	BNL	8	$ -	$ -	0%	$ -
ADC	IBM	ADC	IBM	80	$ -	$ -	0%	$ -
Serializer	Peregrine	Serializer	Peregrine	20	$ -	$ -	0%	$ -
Interface ASIC	IBM	Multiplexer between ADC and Serializer	IBM	20	$ -	$ -	0%	$ -
Optical Module	SMU	Optical Module	SMU	20	$ -	$ -	0%	$ -
Cooling Plate	Custom	Cooling Plate	Custom	2	$ -	$ -	0%	$ -
LTM4616	Linear	Point of Load Converter	Digikey	6	$ 23.62	$ 141.72	20%	$ 28.34
LTM4619	Linear	Point of Load Converter	Digikey	6	$ 20.34	$ 122.04	20%	$ 24.41
TPS74401	TI	LDO Regulator	Digikey	8	$ 5.50	$ 44.00	20%	$ 8.80
5352068-1	TE	Type A Right Angle 2mm HM Connector	Digikey	3	$ 6.97	$ 20.92	20%	$ 4.18
5352152-1	TE	Type B Right Angle 2mm HM Connector	Digikey	3	$ 7.24	$ 21.71	20%	$ 4.34
5338108-2	TE	Type A Lower Shield	Digikey	3	$ 2.07	$ 6.22	20%	$ 1.24
352468-2	TE	Type B Lower Shield	Digikey	3	$ 4.92	$ 14.76	20%	$ 2.95
KS10-0002	Hypertronics	10-pin Right Angle Power Connector	Hypertronics	1	$ 25.78	$ 25.78	20%	$ 5.16
84517	FCI	FCI Meg-Array Connector	Digikey	16	$ 10.56	$ 168.96	20%	$ 33.79
Front Panel	Many	Front Panel Assembly	Many	1	$ 35.00	$ 35.00	20%	$ 7.00
Misc (Resistor, Capaci	Rohm/AVX	SMT Chip Resistor/Ceramic Capacitor	Digikey	10000	$ 0.02	$ 200.00	20%	$ 40.00
						$ 1,736.11	36%	$ 627.72
Total Cost				150		$ 260,416.22	36%	